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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,010	08/22/2003	Timothy E. Hoglund	03-0084	8967

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LSI Logic Corporation
Corporate Legal Department, M/S D-106
Intellectual Property Services Group
1551 McCarthy Boulevard
Milpitas, CA 95035

EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,010	HOGLUND ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 2, 5, 6, 7, 8, 9, 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callway (US 6,950,772 B1) in view of Conner (US 4,450,560).

As per claim 1, Callway teaches a method for observing the state of internal signals during chip testing, comprising: receiving specific test signals in at least one module in order to form a plurality of test signals; combining the specific test signals received to create the plurality of test signals; identifying specific test signals in order to form a plurality of output test signals; and mapping the specific test signals identified to create the plurality of output test signals (fig. 2, 3, abstract, col. 3, lines 49-57, col. 6, lines 28-52, Callway).

However Callway does not explicitly teach the specific use of test signal groups.

Conner in an analogous art teaches a group sequence generator for causing the format and timing generator to provide updated format and timing information corresponding to groups of the test signals and the standards for testing the memory devices (col. 1, lines 55-59, Conner).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Callway's patent with the teachings of Conner by including an additional step of using the test signal groups.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the test signal groups would provide the opportunity to simultaneously analyze the test signals.

- As per claim 2, Callway and Conner teach the additional limitations.

Callway teaches the method wherein the at least one module includes a plurality of modules (fig. 2, col. 3, lines 54-57, Callway).

- As per claim 5, Callway and Conner teach the additional limitations.

Callway teaches the method wherein combining the specific test signals received for each test signal group to create the plurality of test signals is performed by a multiplexer (fig. 2, col. 3, lines 60-63, Callway).

Conner teaches test signal groups (col. 1, lines 55-59, Conner).

- As per claim 6, Callway and Conner teach the additional limitations.

Callway teaches the method wherein mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups is performed using byte lane mapping logic (col. 6, lines 43-47, Callway).

- As per claim 7, Callway and Conner teach the additional limitations.

Callway teaches an apparatus for observing the state of internal signals during chip testing, comprising: multiplexing means for combining test signals in a module to create specified test signals; mapping means for mapping specified test signals to specified test output signals (fig. 2, 3, abstract, col. 3, lines 49-57, col. 6, lines 28-52, Callway).

Conner teaches test signal groups (col. 1, lines 55-59, Conner).

- As per claim 8, Callway and Conner teach the additional limitations.

Callway teaches a system for observing the state of internal signals during chip testing, comprising: means for receiving specific test signals in at least one module in order to form a plurality of test signals;

means for combining the specific test signals received for each test signal to create the plurality of test signals; means for identifying specific test signal in order to form a plurality of output test signals; and means for mapping the specific test signals identified for each test signal output to create the plurality of test signal outputs (fig. 2, 3, abstract, col. 3, lines 49-57, col. 6, lines 28-52, Callway).

Conner teaches test signal groups (col. 1, lines 55-59, Conner).

- As per claim 9, Callway and Conner teach the additional limitations.

Callway teaches the system wherein the at least one module includes a plurality of modules (fig. 2, col. 3, lines 54-57, Callway).

- As per claim 12, Callway and Conner teach the additional limitations.

Callway teaches the system wherein the means for combining the specific test signals received for each test signal to create the plurality of test signals is a multiplexer (fig. 2, col. 3, lines 60-63, Callway).

Conner teaches test signal groups (col. 1, lines 55-59, Conner).

- As per claim 13, Callway and Conner teach the additional limitations.

Callway teaches the system wherein the means for mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups is performed using byte lane mapping logic (col. 6, lines 43-47, Callway).

4. Claims 3, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callway (US 6,950,772 B1) and Conner (US 4,450,560) as applied to claim 2 above, and further in view of Swart (US 5,389,885).

As per claim 3, Callway and Conner substantially teach the claimed invention described in claim 2 (as rejected above).

However Callway and Conner do not explicitly teach the specific use of the method, further comprising: concurrently observing test signals for a plurality of modules.

Swart in an analogous art teaches that electrical test signals...under test (col. 8, line 65 to col. 9, line 2, Swart).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Callway's patent with the teachings of Swart by including an additional step of using the method, further comprising: concurrently observing test signals for a plurality of modules.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method, further comprising: concurrently observing test signals for a plurality of modules would provide the opportunity to compare test signals output from different modules and analyze the signals.

- As per claim 10, Callway, Conner and Swart teach the additional limitations.

Swart teaches the system, further comprising: concurrently observing test signals for a plurality of modules (col. 8, line 65 to col. 9, line 2, Swart).

5. Claims 4, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callway (US 6,950,772 B1), Conner (US 4,450,560) and Swart (US 5,389,885) as applied to claim 3 above, and further in view of Moore et al. (US 5,604,432).

As per claim 4, Callway, Conner and Swart substantially teach the claimed invention described in claim 3 (as rejected above).

However Callway, Conner and Swart do not explicitly teach the specific use of the method, wherein the plurality of modules includes identical modules.

Moore et al. in an analogous art teach that it is desirable to be able to use the same test vectors for identical modules (col. 4, lines 43-44, Moore et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Callway's patent with the teachings of Moore et al. by including an additional step of using the method, wherein the plurality of modules includes identical modules.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method, wherein the plurality of modules includes identical modules would provide the opportunity to compare the test signal output simultaneously from the identical modules.

- As per claim 11, Callway, Conner, Swart and Moore et al. teach the additional limitations.

Moore et al. teach the system wherein the plurality of modules includes identical modules (col. 4, lines 43-44, Moore et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

GUY LAMARRE
PRIMARY EXAMINER